

REMARKS

Claims 1-7 and 15-21 are cancelled without prejudice, claims 8, 9, 11, 12, 13, and 14 are amended to further claim the invention, and new claims 22-32 are added to claim the invention in alternative language. Claims 8-14 and 22-32 remain for consideration and are thought to be allowable over the cited art.

Independent claim 8 as amended clarifies that first and second source code definitions of separate data structures are used to generate instances of the common software tile and instances of the unique software tiles (e.g., paragraphs [0037] - [0038]). New independent claim 22 includes similar limitations. These limitations are not apparent in the prior art.

New claims 22-32 are thought to be patentable over the prior art because the combination of limitations is not understood to be shown or suggested. New independent claim 22 includes limitations similar to those of claim 8 and is understood to be patentable for the reasons set forth above. Claims 23-28, which depend from claim 22, are patentable as depending from a patentable base claim.

New independent claim 29 is directed to a processor-based method for representing resources of a field programmable gate array (FPGA). The method includes establishing in a computer memory, a plurality of instances of a first type tile from a source code specification of the first type tile. The source code specification of the first type tile specifies a programmable switch matrix, a first set of pins for coupling to instances of the first type tile, and a second set of pins. A respective plurality of instances for each of the plurality of unique types of tiles is also established in a computer memory. The plurality of instances of the unique types of tiles are established from respective source code specifications of a plurality of unique types of tiles. Each source code specification of a unique type tile specifies a set of logic resources that is different from sets of logic resources of all other of the plurality of unique types of tiles and a set of pins for coupling an instance of the unique type tile to an instance of the first type of tile. The source code specifications of the plurality of unique types of tiles and of the first type of tile are separate data structure definitions. This combination of limitations is neither shown nor suggested by the prior art, and claims 29-32 are therefore understood to be patentable. Support for the new claims

may be found in paragraphs, [0031], [0032], [0035], [0036], [0037], [0038], [0040], [0047], and [0061], for example.

The Office Action does not show that claims 1-21 are anticipated under 35 U.S.C. 102(e) by "Agrawal" (US Patent Application No. 2004/0010767 to Agrawal et al.). The rejection is respectfully traversed for the reasons set forth in the response dated January 11, 2006. In view of the amendments to the claims, however, the rejection is now moot and should be withdrawn.

Conclusion

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested. If any action other than allowance is contemplated by the Examiner, the Examiner is respectfully requested to telephone Applicants' agent, Lois D. Cartier, at 720-652-3733.

Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on April 11, 2006.

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Signature